(12) UK Patent Application (19) GB (11) 2 106 714 A

(21) Application No 8213035
(22) Date of filing 6 May 1982
(30) Priority data
(31) 305488
(32) 25 Sep 1981
(33) United States of America (US)
(43) Application published 13 Apr 1983
(51) INT CL[3] H01G 1/147
(52) Domestic classification H1M 1B2BX 1G12 1M DX
(56) Documents cited
GB 1425211
GB 1406509
GB 1139609
Vacuum Deposition of Thin Films by L Holland published by Chapman and Hall 6th Printing pages 531 et seq
(58) Field of search H1M

(71) Applicants
AVX Corporation,
(USA-Delaware),
60 Cutter Mill Road,
Great Neck,
L.I. New York 11022,
United States of America.
(72) Inventors
Kim Ritchie,
Elliott Philofsky.
(74) Agents
F.J. Cleveland and Company,
40-43 Chancery Lane,
London WC2A 1JQ.

(54) **Ceramic capacitor and method of making the same**

(57) A ceramic capacitor comprises alternate layers of ceramic dielectric material (11) and electrode layers (12, 13) interposed between the ceramic layers (11), alternate ones of the electrode layers (12, 13) having edge portions extending to and being exposed respectively at first and second opposite margins (14, 15) of the capacitor, the first and second margins being coated by a sputter deposited metallic layer (18) bonded to the exposed ceramic components of the margins and to the exposed portions of the electrode layers whereby two terminals are provided, the exposed electrode edges on a respective margin are electrically inter-connected and the components of the margins (14,15) are mechanically bonded. The margins (14,15) may be first prepared by sputter etching to give a roughened surface (19) for the layer (18). The layer (18) may be of nickel or nickel-vanadium alloy and may comprise a plurality of sub-layers, eg. chromium, nickel, silver, each applied by sputter deposition.

FIG.4A

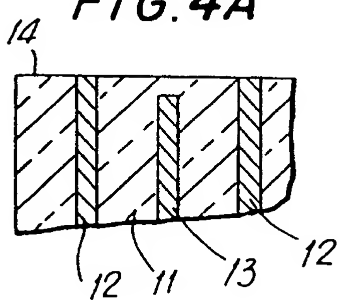


FIG.4B

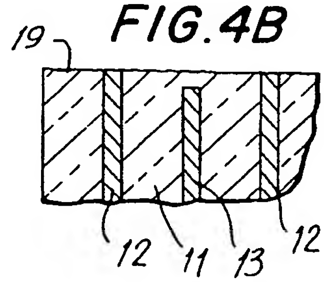
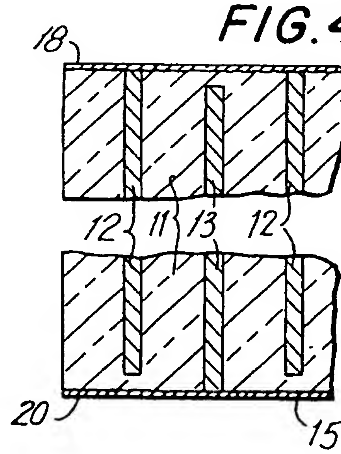


FIG.4C



BEST AVAILABLE COPY

GB 2 106 714 A

2106714

FIG.1

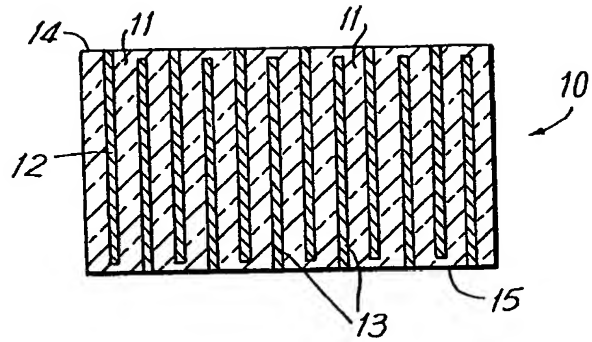


FIG.2

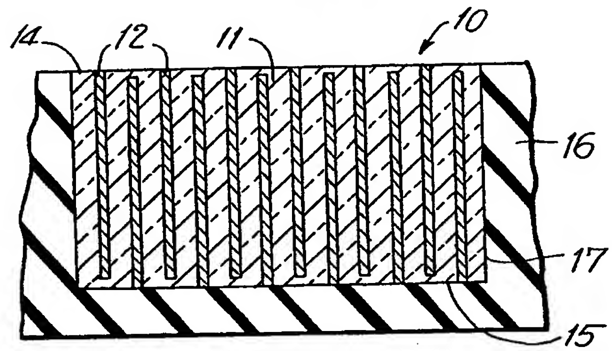


FIG.3

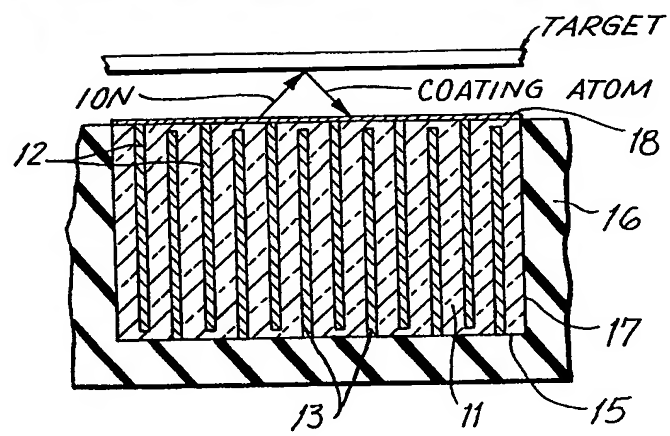


FIG.4A

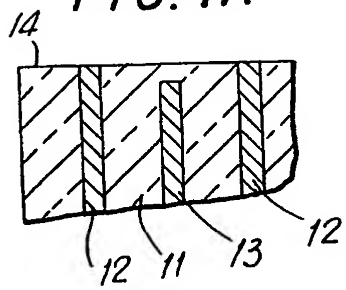


FIG.4B

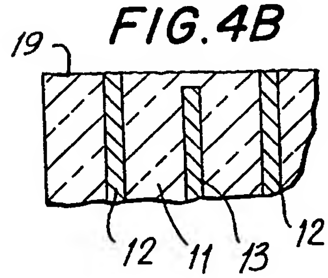
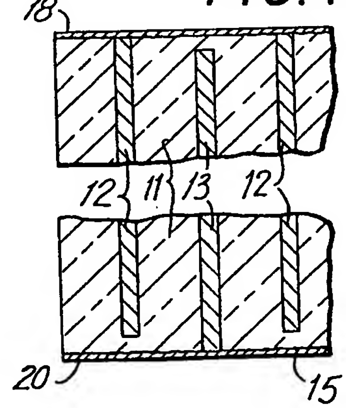


FIG.4C



SPECIFICATION

Ceramic capacitor and method of making the same

Background of the invention

Field of the invention

The present invention relates to ceramic capacitors and more particularly pertains to an improved ceramic capacitor and method of making same. More particularly, this invention relates to a novel method of effecting termination of a fired ceramic capacitor device and to the resultant improved capacitor device.

The prior art

The manufacture of ceramic capacitors is described generally in one or more of the following U.S. Letters Patent:

3,004,197	October 10, 1961
3,235,939	February 22, 1966

Generally speaking such method involves forming a sheet or sheets of green ceramic comprising in essence ceramic powder material in an organic binder. The sheets are imprinted by silk-screening or a similar process with an ink incorporating metal particles resistant to disintegration at high temperatures. A multiplicity of such sheets are stacked with the imprinted or electrode forming areas in partial registry. The stacked sheets are then cut into discrete increments along severence lines, such that the increments expose alternate electrode layers at opposite edge margins.

The increments are next treated by heating to a first temperature for a time sufficient to burn off the organic binder materials. Heating is then continued at a higher temperature to fire the ceramic and to cause the electrode imprinted areas to form conductive metallic electrodes between the ceramic layers.

The resultant ceramic capacitor subcomponents must now be terminated i.e. a conductive connection must be effective between the edges of the various electrode layers exposed at the opposite margins of the capacitor preform.

Heretofore, such connections have been effected by applying a silver containing paste to the respective margins and heating the capacitor to cause the silver to sinter whereby the electrodes at the respective margins are interconnected.

In some cases, conductive leads are soldered to the silver terminations. More typically, particularly with capacitors of small value, the capacitors are coated with a protective insulating coat in all areas except the termination and are shipped for use in such condition.

Obviously, the cost of such silver terminated leadless capacitors is substantially increased as a result of the necessity of employing considerable amounts of silver in effecting termination. The silver terminated capacitors are further disadvantageous, in that, when a soldered connection is made to the silver termination the silver tends to dissolve and flow into the lead-tin alloy of the solder. Unless such soldering is carefully effected, the silver of the termination joint may flow so completely into the solder as to partially or completely lose electrical contact with the electrode layers.

A further disadvantage of conventionally terminated ceramic capacitors is that the silver termination is of little structural value in reinforcing the capacitor against delamination since the sole or principle adherance of the silver is to the electrode materials per se and not the ceramic. In order to provide a degree of reinforcing effect certain of the silver terminating pastes may embody glass frit material which forms a partial bond to the ceramic. However, the utilisation of glass frit material engenders other difficulties and manufacturing complications including the requirement of heating the units up to a temperature sufficiently high to melt the frit component of the silver paste. The high heat requirements of the procedure in addition to being energy wasteful also increase the chances that the capacitors will be damaged in the course of reheating. Finally, the conductivity of the silver-frit termination paste in inferior to a pure metallic conductive material.

Summary of the invention

The present invention may be summarized as directed to an improved method of manufacturing ceramic capacitors and to an improved resultant capacitor. In accordance with the method of the invention a conventional chip capacitor which has been fired is loaded into a jig or like masking device which exposes only the edge margin surfaces of the capacitor which incorporates the edge portions of the electrodes. The masked capacitors are placed in a sputtering apparatus known per se wherein heavy gas ions are impacted against a target material resulting in atoms of the target material being bombarded against the exposed surface of the capacitor. Optionally, but preferably, the exposed surface of the capacitor, prior to sputtering, is itself R.F. suptter etched i.e. the heavy gas ions are impacted directly against the exposed surface of the capacitor. Such sputter etching in addition to removing the oxides or impurities at the surface provides a rugose or corrugated surface for the subsequent sputter applied metallic layer.

In accordance with the method more than one sputter applied metallic layer may be deposited on the capacitor surface in accordance with the intended end use of the capacitor. By way of example a satisfactory

capacitor termination may be effected by sputter depositing a nickel layer, an alloy of nickel vanadium, a copper layer etc. Optionally, a chromium layer may first be deposited to improve adhesion followed by a nickel or nickel vanadium sputter applied layer. To facilitate subsequent soldering a very thin silver layer may be applied over the nickel e.g. in the order of .1 micron.

The capacitor in accordance with the invention provides a highly desirable structure in that the absence of silver at the junction with the capacitor electrodes eliminates the possibility that electrode contact will be lost in the course of soldering. Substantial cost reductions are achieved by eliminating the use of silver terminations. Additionally and importantly, the sputter deposited layer, particularly if the edge portion of the capacitor has been previously sputter etched, provides a coating which adheres strongly both to the electrodes and to the intervening ceramic spaces whereby any tendency of the capacitor to delaminate along the cleavage lines defined by the ceramic-electrode interfaces is substantially reduced or eliminated. The mechanical reinforcing effect of the sputter deposited terminations enables the final insulating or incapsulating coating, if used, to function merely as an electrical isolation rather than as a mechanical reinforcement of the capacitor. Thus the overall size or bulk of the capacitor may be reduced.

It is accordingly an object of the invention to provide an improved method of fabricating a ceramic capacitor and more particularly an improved method of terminating a conventional ceramic capacitor. A further object of the invention is the provision of a novel termination method for ceramic capacitors which eliminates the use of silver or other noble metals at the interface with the capacitor electrodes. Still a further object of the invention is the provision of a method of fabricating ceramic capacitors which includes the step of sputter etching the electrode containing margin of the capacitor to clean the same and provide an etched or pebbled surface and thereafter sputter depositing a thin film of conductive metal which simultaneously electrically unites the exposed electrodes and forms a unifying or mechanically rigidifying influence at the capacitor margin.

A further object of the invention is the provision of a ceramic capacitor having termination which are free of silver at the interface with the electrodes. A further object of the invention is the provision of a capacitor of the type described wherein the termination layer functions as a mechanical reinforcement against delamination of the capacitor. Still other and further object of the invention will appear herein of be hereinafter pointed out in connection with the description of the drawings wherein.

Figure 1 is a vertical sectional view diagrammatic in nature of a ceramic capacitor preparatory to termination.

Figure 2 is a view similar to Figure 1 showing the capacitor in a masking apparatus.

Figure 3 is a diagrammatic view of the masked capacitor in the course of sputter deposition treatment.

Figures 4A, 4B and *4C* are diagrammatic sequential views respectively of an untreated capacitor, a capacitor which is sputter etched on its upper surface, and of a capacitor having a sputter deposited layer covering the sputter etched surface.

As used herein the term sputter coating, sputter depositing or sputtering shall mean the gas ion disentegration of a cathode target and consequent deposition of atoms removed from the target as a layer on the capacitor margin having exposed electrode edges.

The term sputter etching or sputter etched shall be deemed to mean a procedure whereby cathode and gas ions are directed against the capacitor margins to be terminated in an R.F. field.

Turning now to the drawings there is shown in Figure 1 in diagrammatic form a ceramic capacitor conventional in nature and fabricated for instance in accordance with the disclosures of U.S. Patent 3,235,939. The capacitor 10 comprises a multiplicity of ceramic layers 11 defining the dielectric components of the capacitors, the layers 11 being separated by intervening electrode layers 12 and 13.

As is conventional the electrode layers 12 and 13 extend for less than the entire length of the capacitor but overlap throughout the majority of their extent. As is apparent from Figure 1 the electrode layers 12 incorporate edge portions which are exposed at the margin 14 of the capacitor 10 whereas the electrodes 13 include edge portions exposed at the margin 15 of the capacitor.

In accordance with the process of the invention a multiplicity of the capacitors 10 are loaded into a die or jig 16 (Figure 2) the function of which is to shield all of the surfaces of the capacitor except the uppermost surface i.e. one or the other of the marginal surfaces 14 or 15. As depicted in Figure 2 the marginal surface 14 of the capacitor is located uppermost in the mask of jig 16. It will accordingly be appreciated that the edge portions of the electrodes 12 are exposed in an upward direction.

Although in the diagramatic views of the Figures 1 through 3 the capacitors 10 have been depicted as shielded by individual pockets 17 of the masking device 16, it will be understood that a mutual shielding effect may be achieved by stacking a multiplicity of the capacitors in side by side relation.

The shielded capacitors are next processed by sputter etching the uppermost surface or margin 14. While the sputter etching step is optional such step is preferred, in that, in addition to the usual effect of cleaning the exposed surface, the sputter etching step also provides a rugose or corrugated or pebbled impact area for the subsequently applied metallic layer. The effect of sputter etching is diagrammatically illustrated by a comparison of Figure 4A (unetched) with 4B (sputter etched).

The sputter etched surface 14 is next sputter coated by passing the same beneath the target of a sputtering device. Optionally, but preferably, an in-line sputtering system such as a system identified as the SERIES 900 SPUTTERING DEVICE as manufactured by Materials Research Corporation of Orangeburgh, New York is employed. An inline sputtering system is advantageous in that it permits the capacitors to be progressively

advanced beneath target areas of different compositions whereby a layer of a first sputter deposited material may be formed directly over the surface 14 and thereafter a second sputter deposited layer may be formed over the first layer. Illustratively, a nickel-vanadium alloy layer may first be sputter deposited by advancing the capacitor beneath an appropriate target material, the nickel or nickel-vanadium layer being thereafter thin coated with a silver layer by advancing the same beneath a silver target member. It is also desirable under certain circumstances i.e. for improved adhesion, to first effect the deposition of a thin chromium layer and thereafter coat the chromium layer by sputter deposition with a nickel or nickel-vanadium layer, such procedures being readily carried out in an inline sputtering system by progressively advancing the capacitors beneath suitably selected target materials.

The sputter deposition is continued in a manner known per se until the desired layer build up is achieved. Referring to Figure 4C it will be apparent that the sputter deposited layer or layers 18 will define a cohesive mass of layer, the lowermost surface of which is strongly adherent to and enters within the recesses, interstices or pores 19 formed by the sputter etching procedure. The layer 18 provides an effective electrical and mechanical connection to the electrodes 12 and a mechanical connection to exposed ceramic components at the surface 14. The layer 18 thus provides a termination and a mechanical reinforcement of the edge 14 minimizing the possibility of cleavage of the capacitor along the lines of interface between the ceramic and electrodes.

It will be appreciated that the etching and sputtering procedures described are repeated with the edge portion 15 of the ceramic exposed to the target whereby a second termination layer 20 is formed over the edge 15.

The terminated capacitor is now ready for use. Optionally, an insulating coating may be applied over all portions of the capacitor except the terminations.

By way of example, and for purposes of compliance with the requirements of the patent laws, there will now be described the operating parameters of a specific embodiment of the invention it being understood that neither the materials nor the specific details of such description shall be considered limitative.

In accordance with the invention a multiplicity of chips are located in a fixture with the termination ends exposed in a upward direction. The loaded fixture is placed in a vacuum load lock which is pumped to a pressure of less than 50×10^{-3} torr prior to introducing the fixture into the main vacuum sputtering chamber. The loaded fixture is moved to an R.F. sputter etching station wherein the pressure is less than 5×10^{-6} torr. A high purity argon gas is introduced into the etching chamber to achieve a pressure of about 10×10^{-3} torr. The parts having a surface area of approximately 311 millimeters square are sputter etched for 30 seconds at a power level of 1.4 kilowatt. The fixture carrying the etched capacitors is then traversed to a station where a .12 micrometer thickness film is deposited over the termination end. The film may comprise pure nickel or an alloy containing by weight 93% nickel and 7% vanadium. Sputtering is effected at a power level of 4.2 kilowatts and a scan speed of 10.2 millimeters per second across the target area. The sputtering is preformed in a argon gas environment at a pressure 10×10^{-3} torr. The procedure is repeated to effect etching and coating of the opposite termination surface of the capacitors.

Where direct nickel or nickel-vanadium coatings are effected, coating thickness in the range of from .12 to .5 micrometers has been found to be optimum. Where a chromium substrate is used for high adhesion, layer thicknesses in the range of .02 to .05 micrometers have been found preferred. As previously noted where direct soldering to the terminations is anticipated a very thin coating of silver i.e. of the magnitude of about .1 micron is desirably added. It will be observed that such quantity of silver is only a very small fraction of the amount typically used to terminate a capacitor by conventional methods.

From the foregoing it will be perceived that there is provided in accordance with the present invention a new and novel method of manufacturing ceramic capacitors characterized in that the termination step is effected by sputter deposition preferably following sputter etching. It will further be perceived that the resultant unique capacitor may be economically manufactured and is uniquely strong and free from the tendency toward silver leaching during soldering which is characteristic of conventional silver terminated capacitors.

As will be apparent to those skilled in the art, numerous changes may be effected particularly in the selection of materals, layer thicknesses and treatment parameters for effecting etching and coating. Accordingly, the invention is to be broadly construed within the scope of the appended claims.

CLAIMS

1. As a new article of manufacture a ceramic capacitor device comprising alternate layers of ceramic dielectric material, layers of electrode material interposed between said ceramic layers, alternate ones of said electrode layers having a first edge portion extending to and being exposed respectively at first and second opposite margins of said capacitor, the edges of said electrode layers opposite said first edge portions terminating short of said margins, said capacitor being characterized in that said first and second margins of said capacitor are coated by a sputter deposited metallic layer, said layer being bonded to the exposed ceramic components of said margins and to the exposed edge portions of said electrode layers whereby the layers exposed at said edges are electrically connected and the ceramic and electrode components of said edge portions are mechanically bonded, said deposited metallic layers in addition defining terminations of said capacitor.

2. A capacitor in accordance with claim 1 wherein said margin portions have been sputter etched to provide a rugose surface prior to deposition of said metallic layer whereby the material of said sputter deposited layer enters the interstices in said ceramic and electrode materials to thereby form a destratification resistant bond with said layers as well as a mechanical and electrical bond to said exposed portions of said electrodes.

3. A capacitor in accordance with claim 2 wherein said layer comprises nickel.

4. A capacitor in accordance with claim 2 wherein said layer comprises chromium, the combination including a second sputter deposited metallic layer covering said first layer.

5. A capacitor in accordance with claim 4 wherein said second layer comprises nickel.

6. A capacitor in accordance with claim 3 and including a sputter deposited silver layer covering said nickel layer.

7. A capacitor in accordance with claim 6 wherein said silver layer is of a thickness of about .1 micron.

8. The method of manufacturing a ceramic capacitor device which includes interposing between alternate layers of a green ceramic, layers of electrode material, alternate ones of said electrode layers having a first edge portion extending to and being respectively at first and second opposite margins of said device, the edges of said electrode layers opposite said first edge portions terminating short of said margins, firing said green ceramic and, thereafter, sequentially positioning said first and then said second marginal portions of said fired capacitor within a sputtering zone in predetermined spaced relation to a metallic target cathode while shielding all but said marginal portion to be sputtered whereby an electrically conductive sputtered layer of target material is caused to be bonded to the ceramic and to the exposed electrode areas defining said marginal portion to thus electrically connect the electrode layers of the treat-treated margin said sputtered layers defining terminations of said capacitor.

9. The method in accordance with claim 8 wherein said marginal portions are sputter etched in advance of sputter deposition of said layer to thereby define a rugose surface, the interstices of said surface being filled at least partially by the material of said layer.

10. The method in accordance with claim 9 wherein said layer comprises nickel.

11. The method in accordance with claim 9 wherein said layer comprises chromium and said chromium layer is thereafter covered by a sputter deposited second metallic nickel layer.

12. The method in accordance with claim 9 wherein said layer comprises a nickel-vanadium alloy.

13. The method in accordance with claim 9 and including the step of sputter depositing a silver layer over said metallic layer, said silver layer having a thickness in the order of about .1 micron.

Printed for Her Majesty's Stationery Office, by Croydon Printing Company Limited, Croydon, Surrey, 1983.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.